REMARKS

Specification

In the Office Action, the Examiner objected to claims 1-7, 12 and 13 as failing to set forth the subject matter which Applicants regard as their invention. The Examiner asserted that there is evidence in Applicant's reply filed on November 9, 2005 that claims 1 and 12 fail to correspond in scope with what Applicants regard as their invention. With regard to the objection, the Examiner stated that:

> In that paper [the November 9, 2005 reply], applicant has stated that "The hot carriers are injected into and stored on at least one charge storage dielectric layer **from a drain side of the memory cell,** ..." and also in claims 1 and 12, "... injection of hot carriers from the drain of the memory cell ... effects programming of the memory cell." This statement indicates that the invention is different from what is defined in the specification. Because without clearly defining in the claims that the hot carriers must be "hot holes", paragraph 0046 has clearly indicated that "The substrate bias contributes to the generation and/or acceleration of hot electrons near the drain junction." Therefore, according also to applicants' disclosure, paragraphs 0040 and 0041, these hot carriers (whether primary or even second-impact) are clearly defined as the hot **electrons**, which are" ... attracted towards the gate 5 by the gate voltage and will be **injected near the drain 4 side** of the memory device into the dielectric stack ..." As a result, the description of the programming mechanism, as disclosed in the specification (please read paragraphs 0039-0044 very carefully), contradicts to that of what are claimed and remarked – hot carriers from the drain side. (***Emphasis in original***)

The Examiner's remarks are unclear to Applicants. For instance, the Examiner apparently stated that Applicants should explicitly recite hot-holes in claims 1 and 12 instead of hot-carriers. The Examiner also apparently stated that the specification clearly defines hot-carriers as hot-electrons, which is inconsistent with the assertion that Applicants should recite hot-holes in claims 1 and 12.

Regardless of the clarity of the Examiner's remarks, Applicants respectfully disagree with the Examiner that the claims do not correspond in scope with what Applicants regard as their

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invention. Paragraphs 0039 – 0044 of the specification (which were cited by the Examiner) describe an example embodiment of a programming method for an n-channel memory device, where the hot-carriers that effect programming of the memory device are hot-electrons. However, Applicants also clearly contemplated implementing the programming method recited in the pending claims in a p-channel memory cell, where the hot-carriers that effect programming of the memory cell are hot-holes. For instance, paragraph 0031 of the specification states:

> For purpose of this disclosure, the embodiments discussed herein will be described with respect the use of an n-channel device, for which an n-type drain and n-type source are formed in a p-type substrate or a p-well. However, it will be appreciated that the methods, cell structures and arrays described herein also apply to embodiments employing a p-channel device. Although the device structure shown in FIG. 1 is symmetrical, the term "drain" is used to identify the side of the device from which the memory cell is programmed/erased.

Applicants respectfully submit that one of skill working in this area would, having read the present application, understand that the hot-carriers in claims 1 and 12 are hot-electrons for an n-channel memory device and hot-holes for a p-channel memory device. In both types of memory devices (such as using the symmetrical device of Figure 1 of the application), majority carriers (electrons for n-channel devices and holes for p-channel devices) flow from a source of the memory device to a drain of the memory device and the second-impact hot-carriers (whether it be hot-electrons for an n-channel memory cell or hot-holes for a p-channel memory cell) are generated in the bulk region near the drain of the memory cell.

Embodiments of the method of claim 1 can be applied to the memory device illustrated in Figure 1 of the present application. The device of Figure 1 is a symmetric memory device, which may be implemented as either an n-channel device or p-channel device. Figure 1 is presented below for the Examiner's convenience.

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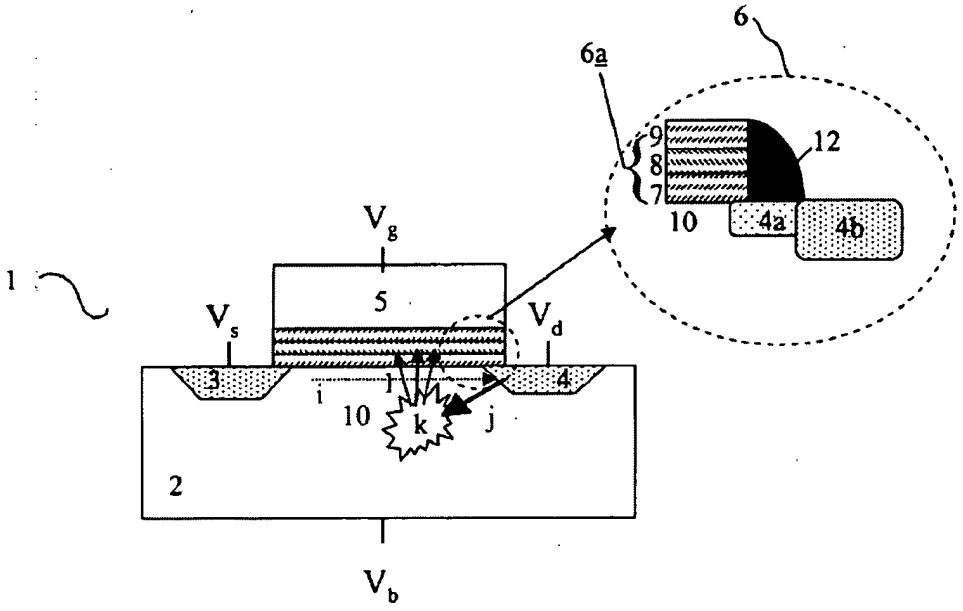

For an n-channel memory device, an embodiment of the method of claim 1 (which is also used to program the memory circuit of claim 12) includes electrons flowing from the source 3 to the drain 4 generally along line "i." At or near the junction of the drain 4, some of the electrons flowing from the source 3 impact (first impact) and create electron-hole pairs. The holes from the created electron-hole pairs (first-impact carriers) then travel (generally along line "j") into the bulk 2 of the memory device. In the bulk 2, some of the first-impact holes impact again (second impact) and create second-impact electron-hole pairs "k." Electrons (e.g., hot-electrons) of the second impact electron-hole pairs are then injected (generally in the directions indicated by the arrows designated "I") into a charge storage dielectric layer 8.

Such an approach for programming an n-channel memory device is described in the present application in paragraphs 0039 – 0044, for example. Applicants note that claims 1 and 12 have been amended to clarify that a majority of the hot-carriers used to program the memory cell (e.g., injected hot-carriers) are generated in the bulk region 2 as a result of secondary impact ionization, as described in the specification.

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One of skill working in this area, after reading the present disclosure (including paragraph 0031, which demonstrates that the programming mechanisms described in the application are applicable to both n-channel and p-channel devices), would be able practice the invention of claims 1 and 12 using either n-channel device(s) or p-channel device(s) without undue experimentation, as the method for programming a p-channel device is substantially the same as the method for programming an n-channel device, where holes take the place of electrons and electrons take the place of holes. Such knowledge is fundamental to a person having ordinary skill in the operation of field effect transistors.

The programming approach recited in claim 1 (and claim 12), when applied to a p-channel memory device includes holes flowing from the source 3 to the drain 4 generally along line "i." At or near the junction of the drain 4, some of the holes flowing from the source 3 impact (first impact) and create electron-hole pairs. The electrons from the created electron-hole pairs (first impact carriers) then travel (generally along line "j") into the bulk 2 of the memory device. In the bulk 2, some of the first impact electrons impact again (second impact) and create second-impact electron-hole pairs "k." Holes (e.g., hot-holes) of the second impact electron-hole pairs are then injected (generally in the directions indicated by the arrows designated "I") into the charge storage dielectric layer 8.

Based on the foregoing, pending claims 1-7, 12 and 13, contrary to the Examiner's objection, do correspond with the subject matter that Applicants regard as their invention. At the time the invention was made, Applicants clearly contemplated the use of second impact hot-electrons and second impact hot-holes for respectively effecting programming of n-type and p-type memory cells. The use of the term "hot-carriers" in the pending claims is, therefore, consistent with the disclosure, as hot-electrons or hot-holes may be used to effect programming

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of a memory cell in conjunction with such methods and memory devices, as contemplated in the disclosure (e.g., in paragraph 0031). Thus, the objection should be withdrawn.

Claim Rejections 35 U.S.C. § 103

Rejections on Lin in view of Eitan

In the Office Action, the Examiner rejected claims 1-7, 12 and 13 under 35 U.S.C. § 103(a) as being obvious over U.S. Patent 6,850,440 to Lin et al. (hereafter "Lin") in view of U.S. Patent 5,768,192 to Eitan. Applicants respectfully traverse this rejection.

Claim 1, as amended, recites:

> A method for programming a single bit nonvolatile memory cell integrated on a metal-dielectric-semiconductor technology chip, the memory cell comprising a semiconductor substrate including a bulk region, a source, a drain, and a channel in the bulk region and in-between the source and the drain; and a control gate that comprises a control gate electrode and a dielectric stack, the control gate electrode being separated from the channel by only the dielectric stack, the dielectric stack consisting of one or more dielectric layers, wherein at least one of the one or more dielectric layers is a charge storage dielectric layer, wherein the method for programming comprises:
>
> applying electrical ground to the source;
>
> applying a first voltage having a first polarity to the drain;
>
> applying a second voltage of the first polarity to the control gate electrode; and
>
> applying a third voltage having a second polarity opposite to the first polarity to the semiconductor substrate,
>
> wherein the first, second and third voltages cooperatively effect programming of the memory cell as a result of injection of hot carriers from the bulk region near the drain of the memory cell, a majority of the injected hot carriers being (i) generated by a secondary impact ionization mechanism (ii) injected into the charge storage dielectric layer and (iii) stored on the charge storage dielectric layer.

Claim 1 is directed to a method for programming a single bit nonvolatile memory cell that is integrated on a metal-dielectric-semiconductor technology chip. The memory cell recited in claim 1 includes a semiconductor substrate including a bulk region, a source, a drain, and a

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channel in the bulk region and in-between the source and the drain. The memory cell recited in claim 1 also includes a control gate, the control gate including a control gate electrode and a dielectric stack, where the control gate electrode is separated from the channel by only the dielectric stack. The dielectric stack consists of one or more dielectric layers, where at least one of the one or more dielectric layers is a charge storage dielectric layer.

An embodiment of a memory cell 1 in accordance with claim 1 is illustrated in Figure 1 of the application. Figure 1 was presented above on page 8 of this response. The memory cell 1 includes a control gate that comprises a control gate electrode 5 (which is a conductive layer – *See* application, page 11, line 23) and a dielectric stack 6a. The control gate electrode 5 is separated from a channel of the memory cell 1 by only the dielectric stack 6a. The dielectric stack 6a consists of three separate dielectric layers 7,8,9, though other arrangements are possible. The dielectric stack 6a shown in Figure 1 is described in the specification on page 13, line 12 through page 14, line 5, which recites:

> The stack 6a of the dielectric layers 7, 8 and 9 may be formed by depositing the first dielectric layer 7 on top of a major surface of the semiconductor substrate 2. The first dielectric layer 7 typically comprises silicon dioxide formed by thermal oxidation of the silicon substrate 2, or can be deposited by a variety of chemical vapor deposition (CVD) techniques. Alternatively, a tetra-ethoxy-silane (TEOS) layer formed by Low Pressure CVD, or oxides formed by Atomic Layer CVD) may be employed. The thickness of the first dielectric layer 7 may be between 3nm and 20 nm, or between 3nm and 10nm. The second dielectric layer 8 is formed on top of the first dielectric 7, which electrically insulates the second dielectric 8 from the channel 10 underneath. For this particular embodiment, the second dielectric layer 8 comprises a silicon nitride layer with a thickness between 2 and 20 nm, or between 5 and 12nm. The third dielectric layer 9 is formed on top of the second dielectric layer 8, e.g. by CVD, which electrically insulates the second dielectric layer 8 from the gate 5. For this embodiment, the third dielectric layer 9 comprises a silicon oxide having a thickness between 3 and 20 nm, or between 3 and 10nm. Such a dielectric layer stack forms an ONO (oxide-nitride-oxide) stack. For this ONO stack, the second dielectric layer 8 (nitride layer) retains the charge used for programming the memory cell 1.

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The foregoing portion of the specification describes the memory cell 1 as including an ONO dielectric stack, where a nitride (silicon-nitride) layer 8 of the ONO stack acts as a charge storage dielectric layer. As recited in claim 1, all of the layers 7,8,9 in the dielectric stack 6a are formed of dielectric materials. Therefore, none of the layers in the dielectric stack 6a are conductive.

In the method of claim 1, as applied to the memory device 1 in Figure 1, second-impact, or secondary hot-carriers (e.g., hot-electrons or hot-holes) are generated by a secondary impact ionization mechanism. These second-impact hot-carriers are then injected into and stored on the charge storage dielectric layer 8. The second-impact carriers are injected from the channel region 10 (in the bulk region 2 of the memory cell 1) near the drain 4 side of the memory cell 1, where the at least one charge storage dielectric layer 8 is included in the dielectric stack 6a. As previously discussed, only the dielectric stack 6a separates the control gate electrode 5 from the channel 10.

In contrast to the memory device of claim 1, Lin discloses floating gate memory cells, such as the memory cell illustrated in Figure 4B of Lin, to which the Examiner cited. The other Figures of Lin cited by the Examiner disclose similar structures. Figure 4B of Lin is included below for the Examiner's convenience.

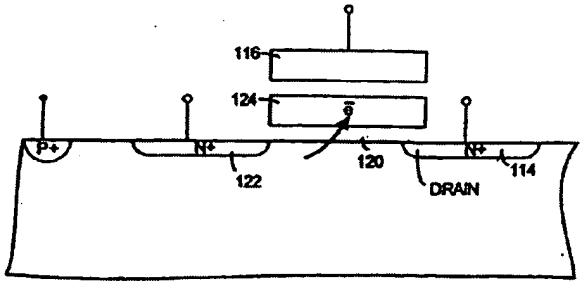

FIG. 4B

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The memory cell shown in Figure 4 includes a polysilicon floating gate structure 124 (*See* column 3, line 45-46) and a word line (control gate) electrode 116. In the Office Action, the Examiner asserted that the floating gate 124 and the top and bottom dielectric layers over and above the floating gate 124 in Figure 4B discloses the dielectric stack 6a of claim 1. As is described in Lin, the floating gate 124 is not a dielectric layer, but is a conductive polysilicon floating gate structure. Because such floating gates are conductive, they do not operate as dielectric materials. Lin, in fact, describes such a floating gate structure in column 6, lines 36-37 as being "made of a suitable conductive material such as doped polysilicon and others."

Because the word line (control gate) electrode 116 of the memory cell in Figure 4B of Lin is separated from the channel of the memory cell by a conductive floating gate, Lin does not disclose a memory device (or a method for programming a memory device) where a control gate electrode of the memory device is separated from a channel of the memory device only by a dielectric stack, where the dielectric stack consists of one or more dielectric layers, as recited in claim 1. The floating gate structure disclosed in Lin would, in operation, result in a substantially different electric field distribution than the control gate structure of claim 1. For instance, the floating gate structure of Lin would operate as a capacitive divider circuit, with the electric field being proportionally distributed between the two dielectric layers (the dielectric layer between the substrate and the floating gate and the dielectric layer between the word line and the floating gate). The control gate structure of claim 1 will not have a capacitive divider effect with all of the applied electric filed being applied across the dielectric stack.

Further, in the method of claim 1, the memory cell is programmed by injecting second-impact hot carriers into a charge storage dielectric layer included in the dielectric stack. In contrast, Lin discloses programming memory cells that include a conductive floating gate

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structure. For instance, programming of the memory cell in Lin's Figure 4B (presented above) is described in column 3, lines 45-46, which recites that programming occurs as a result of "hot electrons [being] injected into the polysilicon (poly 1) floating gate." Therefore, programming of the memory cell of Figure 4B of Lin is accomplished by hot electrons being injected into, and stored on the conductive floating gate 124.

A method for programming a memory cell that includes injecting hot carriers into a conductive floating gate and storing the injected hot carriers on the floating gate (as disclosed in Lin) does not disclose programming a memory cell by injecting hot carriers into at least one charge storage dielectric layer and storing those injected hot carriers on the at least one charge storage dielectric layer (as recited in claims 1 and 12). Therefore, contrary to the assertions made by the Examiner, Lin does not disclose this aspect of claim 1, in addition to the aspects discussed above.

In the Office Action, the Examiner also asserted that:

> Although Lin et al. disclose a method of programming a single bit nonvolatile memory cell as disclosed in claims 1-7, 12 and 13, except the dielectric stack being an ONO stack, wherein a nitride layer is the charge trapping layer, this feature has been taught by Eitan (abstract: ONO trapping dielectric). Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the feature taught by Eitan to the disclosures by Lin et al., so that programming time is greatly reduced (Eitan: abstract).

Applicants respectfully disagree with the Examiner that it would be obvious to combine Lin and Eitan, as there is no suggestion in either Lin or Eitan to combine their teachings. In fact, Eitan teaches away from Lin.

For instance, Eitan describes programming a memory device including a charge trapping layer in column 7, lines 51-59, which recites:

> As previously mentioned, the PROM memory cell 10 is programmed similarly to the prior art PROM memory cell of FIG. 1. Voltages are applied to the gate and

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> drain creating vertical and lateral electrical fields which accelerate the electrons along the length of the channel. As the electrons move along the channel some of them gain sufficient energy to jump over the potential barrier of the bottom silicon dioxide layer 18 and become trapped in the silicon nitride layer 20.

Eitan recites that the programming approach for his memory cell is similar to the approach for the programming of prior art PROM memory cells. Programming of prior art PROM memory cells is described with respect to Figure 1 of Eitan in column 6, lines 12-19, which recites:

> As they [electrons] move along the length of the channel, they gain energy. If they gain enough energy they are able to jump over the potential barrier of the oxide layer 36 into the silicon nitride layer 38 and become trapped. The probability of this occurring is a maximum in the region of the gate next to the drain 34 because it is near the drain that the electrons gain the most energy.

Those of skill working in this area will appreciate that the programming mechanism described in Eitan is a primary hot-carrier injection mechanism. Using such a programming technique, as noted in the portion of Eitan cited above, the location where the highest probability for an electron to jump the potential barrier of the oxide layer 36 is present in the channel next to the drain junction. Therefore, as those working in this area would understand, using primary hot-carrier injection, the injection of charge into a charge storage dielectric layer is concentrated next to the drain in the channel of the memory device being programmed (e.g., in the region where the highest probability of injection exists). The injected charge in such a device would not be distributed in the charge storage dielectric layer (as in the case of a floating gate structure) because the charge storage dielectric layer is non-conductive. Eitan refers to this concentration of injected charge as "localized charge trapping" and describes the benefits of such localized charge trapping as improved programming times. *See* column 6, lines 43-46. Eitan does not appear to suggest or describe the use of other programming approaches and, further, discloses benefits of a primary hot electron injection programming approach.

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Lin, in contrast to Eitan, discloses programming a memory device using second-impact or secondary hot-carrier injection (e.g., channel-initiated secondary electron injection (CHISEL)). The secondary hot-carriers (electrons in Lin) are generated in the channel region (channel-initiated) of a memory device as the result of a secondary impact ionization mechanism. In comparison to Eitan, the hot-carriers used for programming in Lin are generated in the bulk (channel) of the memory device in a region that is offset from drain rather than directly next to the drain. Because the secondary electrons used for programming a memory cell in Lin are generated in the channel (bulk) region of the memory cell, the injection of those secondary electrons onto the floating gate structure of the devices described in Lin will not be concentrated next to the drain junction, as is the case for the programming technique disclosed in Eitan. The secondary electrons will be injected from a larger area of the channel as compared to the injection of primary electrons in Eitan. Further, because the memory cells described in Lin use conductive floating gate structures to store charge, the charge injected to program the memory cell will distribute over the floating gate due to the conductivity of such structures, as opposed to having an area of localized charge trapping in a charge storage dielectric layer, as disclosed in Eitan.

Lin does not suggest, disclose or describe storing charge in a charge storage dielectric layer. Eitan does not suggest, disclose or describe using secondary hot carriers to program a memory cell. Eitan discloses the use of primary hot carrier injection and discusses the benefits of such an approach. Thus, Eitan teaches away from the use of other programming approaches. Based on the foregoing, claim 1 is not obvious over Lin in view Eitan as one of skill in this area would not be motivated to combine Lin with Eitan. Therefore, the rejection of claim 1 should be withdrawn.

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Without addressing the merits of the comments made in the Office Action with respect to claims 2-7, which are not specifically conceded, it is noted that these claims depend from claim 1 and include all of its limitations and the limitations of any intervening claims. The arguments made above with respect to claim 1 apply equally to claims 2-7 and are herein incorporated. Therefore, claims 2-7 are allowable over Lin on the same basis as claim 1 by virtue of claim dependency, and the rejection should be withdrawn.

Claim 12, as amended, recites:

> A memory circuit comprising:
>
> an array of single bit nonvolatile memory cells, each of the memory cells comprising a semiconductor substrate including a bulk region, a source, a drain, and a channel in the bulk region and in-between the source and the drain; and a control gate that comprises a control gate electrode and a dielectric stack, the control gate electrode being separated from the channel by only the dielectric stack, the dielectric stack consisting of one or more dielectric layers, wherein at least one of the one or more dielectric layers is a charge storage dielectric layer;
>
> peripheral circuitry, the peripheral circuitry coupled with the memory cell such that programming of each memory cell is effected using voltages having absolute values of 5 V or less,
>
> wherein the memory cells are programmed as a result of injection of hot carriers from the bulk region near the drain of the memory cell, a majority of the injected hot carriers being (i) generated by a secondary impact ionization mechanism, (ii) injected into the at least one charge storage dielectric layer and (iii) stored on the at least one charge storage dielectric layer.

Claim 12 is directed to a memory circuit that includes an array of memory cells, where the memory cells that are substantially the same as the memory cells described in claim 1 are programmed in a substantially similar fashion as was described above with respect to claim 1. Therefore, claim 12 is not obvious over Lin in view of Eitan for substantially the same reasons discussed above with respect to claim 1, and the rejection should be withdrawn.

Without addressing the merits of the comments made in the Office Action with respect to claim 13, which are not specifically conceded, it is noted that claim 13 depends from claim 12

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and includes all of its limitations. The arguments made above with respect to claim 12 apply equally to claim 13 and are herein incorporated. Therefore, claim 13 is allowable on the same basis as claim 12 by virtue of claim dependency, and the rejection should be withdrawn.

Rejections on Bude in view of Eitan

In the Office Action, the Examiner also rejected claims 1-7, 12 and 13 under 35 U.S.C. § 103(a) as being obvious over U.S. Patent 5,838,617 to Bude et al. (hereafter "Bude") in view of Eitan. This rejection is respectfully traversed.

As was discussed above, claim 1 recites a method for programming a memory cell where hot carriers are injected into and stored on at least one charge storage dielectric layer from a channel in a bulk region near a drain side of the memory cell, where the at least one charge storage dielectric layer is included in a dielectric stack of a control gate and the control gate is separated from the channel by only the dielectric stack. Bude does not disclose or describe such an approach.

In similar fashion as Lin, which was discussed above, Bude is directed to methods of programming floating gate memory devices. Such a floating gate memory device is illustrated in Figure 1 of Bude, which is included below for the Examiner's convenience.

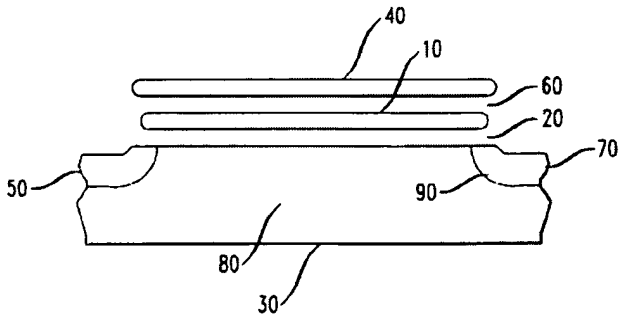

Figure 1

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The floating gate memory device in Bude's Figure 1 includes a conductive floating gate electrode 10 (See column 3, lines 40-42). The floating gate memory device of Bude, in like fashion as Lin, is programmed by injecting secondary hot carriers (channel initiated) into the floating gate electrode 10 and storing the injected hot carriers in the floating gate electrode 10. (See column 3, line 31-35). The arguments made above with regard to Lin apply equally to Bude. Specifically, Bude does not disclose or describe a memory cell where a control gate structure is separated from a channel of the memory cell by only a dielectric stack. Further, Bude discloses programming by injecting hot carriers into a conductive floating gate structure, not by injecting hot carriers into a charge storage dielectric layer, as recited in claims 1 and 12.

As with Lin, Bude does not suggest, disclose or describe the use of a charge storage dielectric and relates only to the programming of memory cells including conductive floating gate structures. Further, in similar fashion as discussed above with respect to Lin and Eitan, there is no motivation to combine Eitan with Bude because Eitan discloses programming a charge storage dielectric layers using primary hot carrier injection, while Bude discloses programming floating gate structures using secondary hot carrier injection. Therefore, claim 1 is not obvious over Bude in view of Eitan for substantially the same reasons discussed above with respect to the rejection of claim 1 over Lin in view of Eitan.

Without addressing the merits of the comments made in the Office Action with respect to claims 2-7, which are not specifically conceded, it is noted that these claims depend from claim 1 and include all of its limitations and the limitations of any intervening claims. The arguments made above with respect to claim 1 apply equally to claims 2-7 and are herein incorporated. Therefore, claims 2-7 are allowable over Bude on the same basis as claim 1 by virtue of claim dependency, and the rejection should be withdrawn.

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As was discussed above with respect to Lin, claim 12 is directed to a memory circuit that includes an array of memory cells. The memory cells of the circuit of claim 12 are programmed as a result of secondary hot carriers being injected into and stored on at least one charge storage dielectric layer. In the memory cells of claim 12, the at least one charge storage dielectric layer is included in a dielectric stack of a control gate. For a given memory cell, a control gate electrode of the control gate is separated from a channel of the memory cell only by the dielectric stack. Therefore, claim 12 is not obvious over Bude in view of Eitan for substantially the same reasons discuss above with respect to claim 1, and the rejection should be withdrawn.

Without addressing the merits of the comments made in the Office Action with respect to claim 13, which are not specifically conceded, it is noted that claim 13 depends from claim 12 and includes all of its limitations. The arguments made above with respect to claim 12 apply equally to claim 13 and are herein incorporated. Therefore, claim 13 is allowable on the same basis as claim 12 by virtue of claim dependency, and the rejection should be withdrawn.

Allowable Subject Matter

Claims 14 and 16 are indicated as being allowable. Applicants respectfully thank the Examiner of this indication of allowability.

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Conclusion

In view of the foregoing, all of the pending claims are in condition for allowance. If the Examiner has any questions, he is invited to contact the undersigned at (360) 379-6514. An early allowance of all the claims is respectfully requested.

Respectfully Submitted,

McDonnell Boehnen Hulbert & Berghoff LLP

Date: Mar. 7, 2006 By: _____

Paul W. Churilla
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CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8

The undersigned hereby certifies that the foregoing RESPONSE TO OFFICE ACTION MAILED ON DECEMBER 8, 2005 is being deposited as first class mail, postage prepaid, in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 7 day of March 2006.

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